IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re patent application of

Francesco A. Campisano et al. Confirmation No.: 8459

Serial No.: 10/079,651 Group Art Unit: 2621

Filed: February 20, 2002 Examiner: D. Czekaj

For: LOW LATENCY VIDEO DECODER WITH HIGH-QUALITY, VARIABLE SCALING AND MINIMAL FRAME BUFFER MEMORY

Commissioner for Patents
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Alexandria, Virginia 22313-1450

APPELLANT'S REPLY BRIEF UNDER 37 C.F.R. §41.41

This reply brief is in response to the Examiner's Answer Mailed January 2, 2008, and replies to arguments made therein.

As pointed out in detail in Appellants' Brief at pages 7 - 12, a distinctive feature of the present invention is the provision of a *variable* frame switch (FS) *point* which is determined (as recited in claim 1, for example, with emphasis added) "in accordance with a signal corresponding to *completion* of *decoding* of a *previous frame*" such that additional time for decoding can be provided without significant increase of latency or corresponding requirement for additional memory in the decoder. The Examiner continues to confuse (perhaps due to the use of the abbreviation "FS" to abbreviate *different* terminology in the present application and Simmons et al., respectively) or at least equate the claimed frame switch *point* (e.g. a point in time), so defined, with a "frame synchronization (FS) *pattern* (66)" of

Simmons et al. which is described at column 5, lines 5 - 28 and 38 - 50 (including the passages relied upon by the Examiner), as being contained within the frame head data 62 of frame 60 (which can also contain "additional frame head data 68" which "may, for example, designate a particular decoding process *to be* used in a *receiver*" (column 5, lines 25 - 29) and, as a "frame head" indicates the *beginning of a frame* such that the frame synchronization *pattern* can be searched for in the (unsynchronized) incoming data and, when detected, can initiate *entry into a decode state* of the receiver for *subsequently* decoding the frame *being received* (column 5, lines 46 - 48). Then, when decoding is complete, the receiver again enters a search mode to, *thereafter*, detect another frame synchronization *pattern*. In short, the frame synchronization pattern of Simmons et al. is a particular code pattern indicating the start of code for a new frame in an unsynchronized data stream. Thus, it is clearly seen that the frame synchronization *pattern* of Simmons et al. *substantively* differs from the (variable, since it is *determined* based on *completion* of *processing* of *previously received* signals, as explicitly claimed) frame switch *point* of the present invention. The frame synchronization *pattern* of Simmons et al. is a *detectable* code *pattern* rather than a *determinable point* in time; indicates the start of *code* for a new frame rather than *completion of decoding* for a *previous frame* (or upon display of a bottom border which the Examiner does not answer); and any signal used in Simmons et al. to indicate completion of decoding of a previous frame merely initiates a search for the next frame synchronization *pattern* in the incoming, unsynchronized code before decoding of the new frame can be started rather than synchronizing decoding in response to the signal indicating completion of decoding of a previous frame, as claimed. In short, there is *no* apparent common characteristic in constitution or function between the claimed frame switch point and the frame synchronization pattern of Simmons et al. while the latter, as disclosed, *cannot* occur at the point in time that the former is determined in the manner claimed.

On page 5 of the Examiner's Answer, the Examiner notes that the claims recite synchronization of the decoder to the display of the bottom border *or* to the frame switch point and then seeks to equate the recitation of the frame switch point to the frame synchronization *pattern* of Simmons et al., noting that upon completion of decoding of a previous frame, the receiver reverts to a search state, which is substantially correct. However, it does not follow (much less logically) from such observations or the further observation that "[s]ince a full frame is decoded based on the detection of an FS pattern, the FS pattern indicates a pont at which different frames occur (where the frames are switched)" that the FS *pattern* of Simmons et al. answers the explicit definition in claim 1 of the determination of the FS *point. In fact, as disclosed by Simmons et al., the time of detection of the FS pattern of Simmons et al. cannot coincide with the completion of decoding of a previous frame since the time of completion of a previous frame is the point at which the search for a subsequent FS pattern is begun and which can therefore only be detected at a later time.* Thus, the time of detection of a frame synchronization pattern in Simmons et al., *since it cannot correspond to the time of completion of decoding of a previous frame,* would not support the meritorious functions of the invention or even provide evidence of a level of ordinary skill in the art which would support the conclusion of obviousness which the Examiner has merely asserted (without providing a compelling line of reasoning but only one which is clearly and logically flawed) since Simmons et al. does not lead to an expectation of success in achieving the meritorious effects of the invention which the use of a frame synchronization pattern in the manner disclosed by Simmons et al. would preclude. Thus, it is also seen that Simmons et al. effectively teaches away from the claimed invention in regard to the claimed frame switch point and its use. Therefore, the Examiner's response to arguments in Appellants' Brief substantively constitute an admission that Simmons et al. does not answer the recitations of claim 1.

Moreover, it is clearly seen that Simmons et al. does not answer *either* of the alternative recitations under the Examiner's analysis which is also believed to be erroneous in view of the subject matter of the invention and does not properly consider the claimed subject matter as a whole since the Examiner effectively ignores the recited synchronization of decoding with a display event (e.g. display of a bottom border of a *scaled* image) since such synchronization *also* provides an advanced start for the decoding process (rather than reduced decoding time, as would otherwise be the case for a scaled image) and reduced latency and requirements for storage in a manner similar to the claimed determination of a frame switch *point*. The Examiner has effectively admitted, by the response to arguments in Appellants Brief that Simmons et al. has nothing to do with synchronizing decoding with any display-related event, much less the display of a bottom border of a scaled image.

In regard to arguments in Appellants' Brief concerning independent claim 9 which is directed to particular testing of spill buffer capacity, the Examiner merely responds (on page 6 of the Examiner's Answer) that Cheney "would have to perform a test", again without benefit of support of any compelling line of reasoning provided by the Examiner and essentially making an improper assertion of inherency. Further, the Examiner asserts that "holding back" operation of the decoder alters decoder latency; which, it is respectfully submitted is not well-taken. Decoder latency is a design consideration in the provision of storage (generally in increments of a number of fields or half frames - see pages 4 - 8 of the present specification) within the decoder for purposes of the decoding process which may make reference to more than one frame and not a merely operational control. Moreover, *both* "scaling *in a decoding path*" *and* "*decoder latency*" are explicitly recited as being altered in response to the claimed test of spill buffer capacity which the Examiner has not addressed.

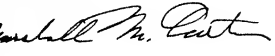
Summary and Conclusion

In view of the foregoing, it is again respectfully submitted that the Examiner continues to fail to make a *prima facie* demonstration of obviousness of any claim in the application. The Examiner's confusion or rationalization in regard to the abundantly evident differences in function and constitution between the claimed frame switch point of the present invention and the frame synchronization pattern of Simmons et al. or in regard to claim construction do not provide evidence upon which a conclusion of obviousness, which the Examiner has asserted without a compelling line of reasoning, can be based. Fundamentally and at best, the Examiner has merely asserted that Simmons et al. might be justified in using the terminology "frame switch" in regard to a signal which is nevertheless merely a detectable code *pattern* and which has nothing to with and cannot predictably correspond in time to a frame switch *point* which is *determined* in accordance with a *signal* corresponding to *completion of decoding or a previous frame* and which supports the derivation of additional time for the decoding process to be completed. Further, the Examiner has not answered the recitations of claim 9 in regard to altering both decoder latency and scaling in the decoder path (e.g. increasing latency while reducing data volume or vice-versa) while improperly asserting inherency and incorrectly equating delay of the decoding function with "decoder latency" (e.g. latency of data *in storage within the decoder*). Therefore, it is respectfully submitted that the Examiner's Answer continues to fail to meet the initial burden of demonstrating that any ground of rejection of record is even arguably proper or supported by evidence in the reference(s) relied upon. Rather, it is respectfully submitted that the Examiner's errors in regard to the grounds of rejection or record are even more evident in view of the Examiner's Answer.

Accordingly, since the claimed subject matter, considered as a whole, is clearly and patentably distinct from the evidence of the level of ordinary skill in the

art determinable from the references relied upon and errors in maintaining the grounds of rejection of record are abundantly evident, it is respectfully submitted that reversal of the Examiner's position in regard to the grounds of rejection of record is in order and such action is respectfully requested.

Respectfully submitted,



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